

# 74ABT16501

## 18-Bit Universal Bus Transceivers with 3-STATE Outputs

### General Description

The ABT16501 18-bit universal bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and  $\overline{OEBA}$ ), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. Output-enable OEAB is active-high. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses  $\overline{OEBA}$ , LEBA, and CLKBA. The output enables are com-

plementary (OEAB is active HIGH and  $\overline{OEBA}$  is active LOW).

To ensure the high-impedance state during power up or power down, OE inputs should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### Features

- Combines D-Type latches and D-Type flip-flops for operation in transparent, latched, or clocked mode
- Flow-through architecture optimizes PCB layout
- Guaranteed latch-up protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

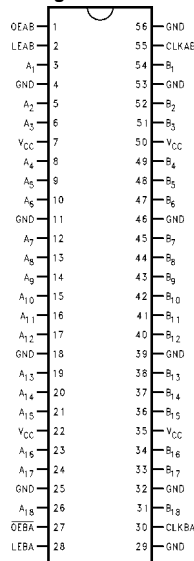
### Ordering Code:

Order Number	Package Number	Package Description
74ABT16501CSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16501CMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape or Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram

Pin Assignment for SSOP



### Function Table (Note 1)

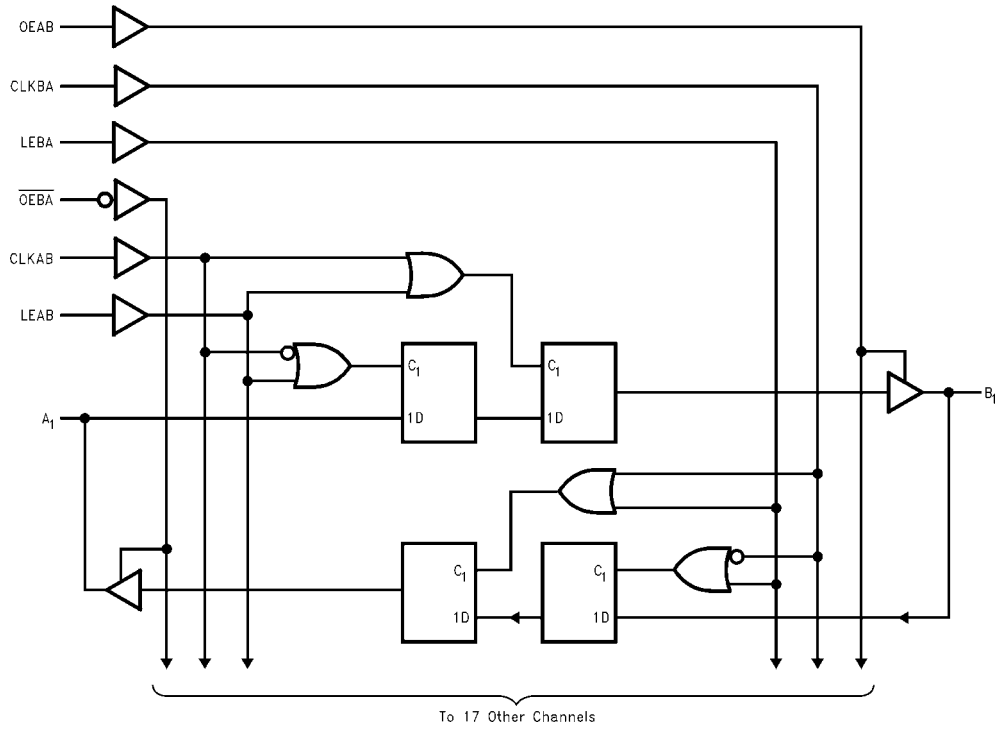
Inputs				Output
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B <sub>0</sub> (Note 2)
H	L	L	X	B <sub>0</sub> (Note 3)

**Note 1:** A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{OEBA}$ , LEBA, and CLKBA.

**Note 2:** Output level before the indicated steady-state input conditions were established.

**Note 3:** Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

Logic Diagram



**Absolute Maximum Ratings**(Note 4)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 5)	-0.5V to +7.0V
Input Current (Note 5)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

DC Latchup Source Current -500 mA  
Over Voltage Latchup (I/O) 10V

**Recommended Operating Conditions**

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
Data Input	50 mV/ns
Enable Input	20 mV/ns

**Note 4:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 5:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.5			V	Min	I <sub>OH</sub> = -3 mA
		2.0			V	Min	I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Output LOW Voltage			0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			1	μA	Max	V <sub>IN</sub> = 2.7V (Note 6)
				1	μA	Max	V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-1	μA	Max	V <sub>IN</sub> = 0.5V (Note 6)
				-1	μA	Max	V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			10	μA	0 - 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}$ , OE = 2.0V
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-10	μA	0 - 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}$ , OE = 2.0V
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.5V; All Others GND
I <sub>CCH</sub>	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			68	mA	Max	An or Bn Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			1.0	mA	Max	$\overline{OE}_n$ = V <sub>CC</sub> , All Others at V <sub>CC</sub> or GND
I <sub>CC1</sub>	Additional I <sub>CC</sub> /Input			2.5	mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 6)	No Load		0.23	mA/ MHz	Max	Outputs Open Transparent Mode One Bit Toggling, 50% Duty Cycle

**Note 6:** Guaranteed, but not tested.

## DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
							C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500Ω
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		0.7	1.2	V	5.0	T <sub>A</sub> = 25°C (Note 7)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-1.5	-1.0		V	5.0	T <sub>A</sub> = 25°C (Note 7)
V <sub>OHV</sub>	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T <sub>A</sub> = 25°C (Note 8)
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage	2.2	1.8		V	5.0	T <sub>A</sub> = 25°C (Note 9)
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage		1.2	0.8	V	5.0	T <sub>A</sub> = 25°C (Note 9)

**Note 7:** Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

**Note 8:** Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

**Note 9:** Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). Guaranteed, but not tested.

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
		f <sub>max</sub>	Maximum Clock Frequency	150	200		
t <sub>PLH</sub>	Propagation Delay	1.0	2.7	4.6	1.0	4.6	ns
t <sub>PHL</sub>	A or B to B or A	1.0	3.2	4.6	1.0	4.6	
t <sub>PLH</sub>	Propagation Delay	1.0	3.1	5.0	1.0	5.0	ns
t <sub>PHL</sub>	LEAB or LEBA to B or A	1.0	3.6	5.5	1.0	5.5	
t <sub>PLH</sub>	Propagation Delay	1.0	3.4	5.3	1.0	5.3	ns
t <sub>PHL</sub>	CLKAB or CLKBA to B or A	1.0	3.7	5.3	1.0	5.3	
t <sub>PZH</sub>	Propagation Delay	1.5	2.7	5.6	1.5	5.6	ns
t <sub>PZL</sub>	OEAB or OEBA to B or A	1.5	3.0	5.6	1.5	5.6	
t <sub>PHZ</sub>	Propagation Delay	1.5	3.7	6.0	1.5	6.0	ns
t <sub>PLZ</sub>	OEAB or OEBA to B or A	1.5	3.2	6.0	1.5	6.0	

## AC Operating Requirements

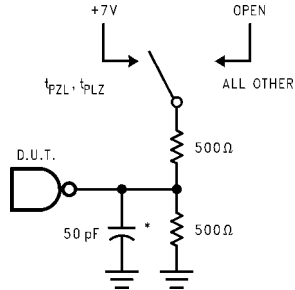
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF		Units
		Min	Max	Min	Max	
		t <sub>S</sub> (H)	Setup Time,	4.0		
t <sub>S</sub> (L)	A to CLKAB, B to CLKBA	4.0		4.0		
t <sub>H</sub> (H)	Hold Time,	0		0		ns
t <sub>H</sub> (L)	A to CLKAB, B to CLKBA	0		0		
t <sub>S</sub> (H)	Setup Time, A to LEAB	4.0		4.0		ns
t <sub>S</sub> (L)	or B to LEBA, $\overline{\text{CLK}}$ HIGH	4.0		4.0		
t <sub>H</sub> (H)	Hold Time, A to LEAB	1.5		1.5		ns
t <sub>H</sub> (L)	or B to LEBA, $\overline{\text{CLK}}$ HIGH	1.5		1.5		
t <sub>S</sub> (H)	Setup Time, A to LEAB	1.5		1.5		ns
t <sub>S</sub> (L)	or B to LEBA, $\overline{\text{CLK}}$ LOW	1.5		1.5		
t <sub>H</sub> (H)	Hold Time, A to LEAB	1.5		1.5		ns
t <sub>H</sub> (L)	or B to LEBA, $\overline{\text{CLK}}$ LOW	1.5		1.5		
t <sub>W</sub> (H)	Pulse Width,	3.3		3.3		ns
t <sub>W</sub> (L)	LEAB or LEBA, HIGH	3.3		3.3		
t <sub>W</sub> (H)	Pulse Width, CLKAB	3.3		3.3		ns
t <sub>W</sub> (L)	or CLKBA, HIGH or LOW	3.3		3.3		

## Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
$C_{IN}$	Input Capacitance	5.0	pF	$V_{CC} = 0.0\text{V}$
$C_{IO}$ (Note 10)	Output Capacitance	11.0	pF	$V_{CC} = 5.0\text{V}$

Note 10:  $C_{IO}$  is measured at frequency  $f = 1\text{ MHz}$  per MIL-STD-883, Method 3012.

## AC Loading



\*Includes jig and probe capacitance.

FIGURE 1. Standard AC Test Load

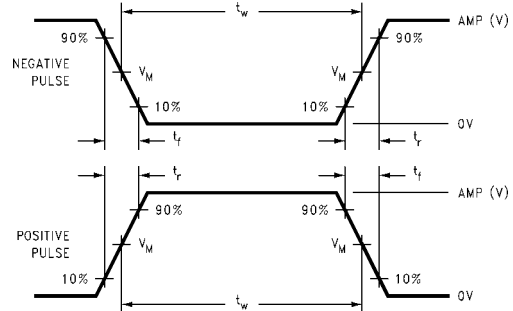


FIGURE 2.  $V_M = 1.5\text{V}$

### Input Pulse Requirements

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

## AC Waveforms

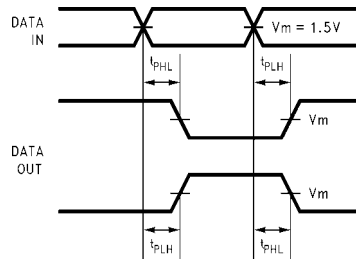


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

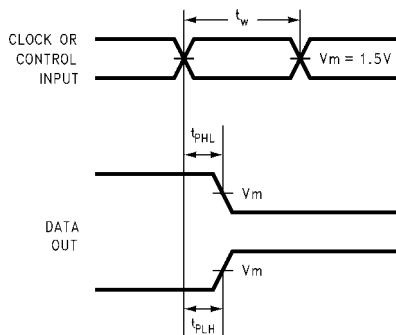


FIGURE 5. Propagation Delay, Pulse Width Waveforms

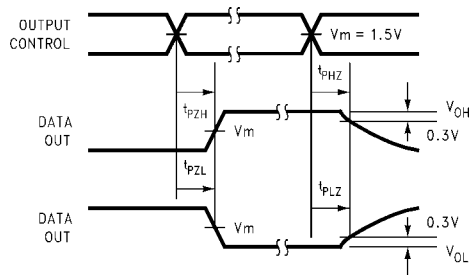


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

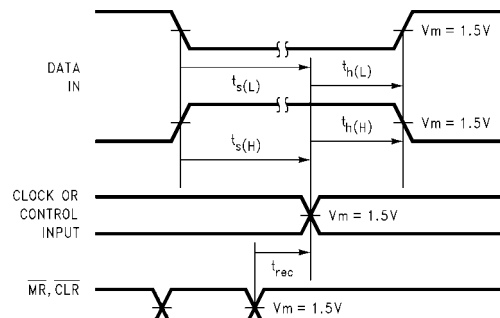
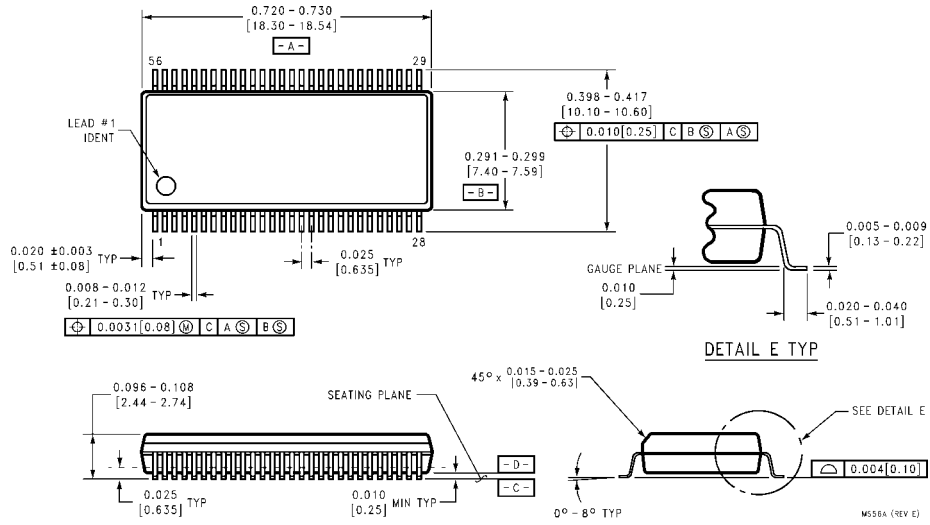


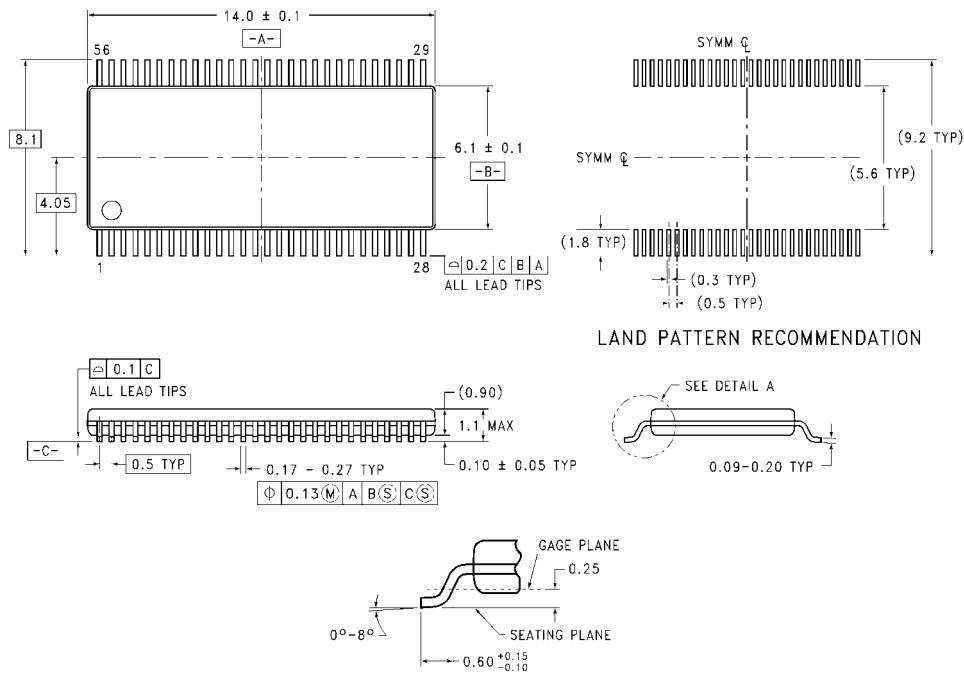
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

**Physical Dimensions** inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS56A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56**

MTD56 (REV B)

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